WHAT IS CLAIMED IS:

1. A dynamic circuit comprising:

a clock input terminal;

a plurality of input terminals;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are connected to one of the plurality of input terminals, respectively,

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and a second potential power supply, and

the precharge MOS transistor is conductive even after formation of a conductive path from the intermediate node to the precharge node.

2. A dynamic circuit comprising:

a first clock input terminal;

a second clock input terminal;

a plurality of input terminals;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the first clock input terminal;

a discharge MOS transistor connecting a source-drain path between a discharge node and a second potential power supply and connecting a gate terminal to the second clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are connected to one of the plurality of input terminals, respectively,

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and the discharge node, and

the precharge MOS transistor is conductive even after formation of a conductive path from the intermediate node to the precharge node.

3. The dynamic circuit according to Claim 1 or 2,

wherein a clock signal applied to the clock input terminal connected to the gate terminal of the precharge MOS transistor is delayed so that the precharge MOS transistor is conducted even after the formation of the conductive path from the intermediate node to the precharge node.

4. The dynamic circuit according to Claim 1 or 2,

wherein a clock signal applied to the clock input terminal connected to the gate terminal of the precharge MOS transistor is produced by performing a logical operation with signals applied to the input terminals so that the precharge MOS transistor is conducted even after the formation of the conductive path from the intermediate node to the precharge node.

5. A dynamic circuit comprising:

a first clock input terminal;

a plurality of input terminals;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the first clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are connected to the plurality of input terminals, respectively, and

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and a second potential power supply,

the dynamic circuit further comprising:

a second clock input terminal; and

a precharge MOS transistor, different from the precharge MOS transistor, connecting the source-drain path between the first potential power supply and the precharge node and connecting the gate terminal to the second clock input terminal,

wherein the different precharge MOS transistor is conductive from the time of formation of a conductive path from the intermediate node to the precharge node.

6. A dynamic circuit comprising:

a first clock input terminal;

a second clock input terminal;

a plurality of input terminals;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the first clock input terminal;

a discharge MOS transistor connecting a source-drain path between a discharge node and a second potential power supply and connecting a gate terminal to the second clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are

connected to one of the plurality of input terminals, respectively, and

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and the discharge node,

the dynamic circuit further comprising:

a third clock input terminal; and

a precharge MOS transistor, different from the precharge MOS transistor, connecting a source-drain path between the first potential power supply and the precharge node and connecting a gate terminal to the third clock input terminal,

wherein the different precharge MOS transistor is conductive from the time of formation of a conductive path from the intermediate node to the precharge node.

7. The dynamic circuit according to Claim 5 or 6,

wherein a clock signal applied to the clock input terminal connected to the gate terminal of the different precharge MOS transistor is delayed so that the different precharge MOS transistor is conducted from the time of the formation of the conductive path from the intermediate node to the precharge node.

8. The dynamic circuit according to Claim 5 or 6,

wherein a clock signal applied to the clock input terminal connected to the gate terminal of the different precharge MOS transistor is produced by performing a logical operation with signals applied to the input terminals so that the different precharge MOS transistor is conducted from the time of the formation of the conductive path from the intermediate node to the precharge node.

9. A dynamic circuit comprising:

a first clock input terminal;

a plurality of input terminals;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the first clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are connected to one of the plurality of input terminals, respectively, and

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and a second potential power supply,

the dynamic circuit further comprising:

a second clock input terminal; and

a precharge MOS transistor, different from the precharge MOS transistor, connecting a source-drain path between the first potential power supply and the precharge node and connecting a gate terminal to the second clock input terminal,

wherein the different precharge MOS transistor is conductive even after formation of a conductive path from the intermediate node to the precharge node.

10. A dynamic circuit comprising:

a first clock input terminal;

a second clock input terminal;

a plurality of input terminals;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the first clock input terminal;

a discharge MOS transistor connecting a source-drain path between a discharge node and a second potential power supply and connecting a gate terminal to the second

clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are connected to one of the plurality of input terminals, respectively, and

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and the discharge node,

the dynamic circuit further comprising:

a third clock input terminal; and

a precharge MOS transistor, different from the precharge MOS transistor, connecting a source-drain path between the first potential power supply and the precharge node and connecting a gate terminal to the third clock input terminal,

wherein the different precharge MOS transistor is conductive even after formation of a conductive path from the intermediate node to the precharge node.

11. The dynamic circuit according to Claim 9 or 10,

wherein a clock signal applied to the clock input terminal connected to the gate terminal of the different precharge MOS transistor is delayed so that the different precharge MOS transistor is conducted even after the formation of the conductive path from the intermediate node to the precharge node.

12. The dynamic circuit according to Claim 9 or 10,

wherein a clock signal applied to the clock input terminal connected to the gate terminal of the different precharge MOS transistor is produced by performing a logical operation with signals applied to the input terminals so that the different precharge MOS transistor is conducted even after the formation of the conductive path from the intermediate node to the precharge node.

13. A dynamic circuit comprising:

a clock input terminal;

a plurality of input terminals;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are connected to one of the plurality of input terminals, respectively, and

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and a second potential power supply,

the dynamic circuit further comprising:

precharge MOS transistors, different from the precharge MOS transistor, smaller than the logical-operating MOS transistors in number,

wherein gate terminals of the different precharge MOS transistors are connected to some of the plurality of input terminals,

source-drain paths of the different precharge MOS transistors are connected between the first potential power supply and the precharge node, and

the first potential power supply and the precharge node is conductive by the different precharge MOS transistors in all cases where the precharge node and the second potential power supply is not conducted and the precharge node and the intermediate node is conducted by the logical-operating MOS transistors.

14. A dynamic circuit comprising:

a first clock input terminal;

a second clock input terminal;

a plurality of input terminals;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the first clock input terminal;

a discharge MOS transistor connecting a source-drain path between a discharge node and a second potential power supply and connecting a gate terminal to the second clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are connected to one of the plurality of input terminals, respectively, and

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and the discharge node,

the dynamic circuit further comprising:

precharge MOS transistors, different from the precharge MOS transistor, smaller than the logical-operating MOS transistors in number,

wherein gate terminals of the different precharge MOS transistors are connected to some of the plurality of input terminals,

source-drain paths of the different precharge MOS transistors are connected between the first potential power supply and the precharge node, and

the first potential power supply and the precharge node is conductive by the different precharge MOS transistors in all cases where the precharge node and the second potential power supply is not conducted and the precharge node and the intermediate node is conducted by the logical-operating MOS transistors.

15. A dynamic circuit comprising:

a first clock input terminal;

a plurality of input terminals;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the first clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are connected to one of the plurality of input terminals, respectively, and

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and a second potential power supply,

the dynamic circuit further comprising:

a second clock input terminal; and

at least one precharge MOS transistor, different from the precharge MOS transistor, connecting a source-drain path between the first potential power supply and the intermediate node and connecting a gate terminal to the second clock input terminal,

wherein the different precharge MOS transistor is made conductive from the time of formation of a conductive path from the intermediate node to the precharge node.

16. A dynamic circuit comprising:

a first clock input terminal;

a second clock input terminal;

a plurality of input terminals;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the first

clock input terminal;

a discharge MOS transistor connecting a source-drain path between a discharge node and a second potential power supply and connecting a gate terminal to the second clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are connected to one of the plurality of input terminals, respectively, and

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and the discharge node,

the dynamic circuit further comprising:

a third clock input terminal; and

a precharge MOS transistor, different from the precharge MOS transistor, connecting a source-drain path between the first potential power supply and the intermediate node and connecting a gate terminal to the third clock input terminal,

wherein the different precharge MOS transistor is conductive from the time of formation of a conductive path from the intermediate node to the precharge node.

17. The dynamic circuit according to Claim 15 or 16,

wherein a clock signal applied to the second clock input terminal is delayed so that the different precharge MOS transistor is conducted from the time of the formation of the conductive path from the intermediate node to the precharge node.

18. The dynamic circuit according to Claim 15 or 16,

wherein a clock signal applied to the second clock input terminal is produced by performing a logical operation with signals applied to the input terminals so that the different precharge MOS transistor is conducted from the time of the formation of the

conductive path from the intermediate node to the precharge node.